Traffic Engineering with Segment Routing: SDN-based Architectural Design and Open Source Implementation

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Overview

• Traditional approaches for Traffic Engineering (TE) require per-flow routing state within all network nodes

• We propose a SDN-based network architecture where per-flow routing states are set-up only at the border of the network
  ➢ TE is implemented through Segment Routing (SE)
  ➢ SDN paradigm is used for performing TE/SR computation and to configure border nodes

• We have designed and implemented a simple SR heuristic for SR path computation

• We have carried out experimental analysis

• We provide an open-source implementation of the proposed architecture
Network Architecture

- ISP network managed by a (logically) centralized SDN controller
- Provider Edge (PE) routers and Core Routers (CR) are hybrid IP/MPLS/SDN nodes (called OSHI nodes and also used in demo)
- MPLS is used for TE
  - TE paths enforced by using Segment Routing (SR)
  - no change to the MPLS forwarding plane is required
  - no MPLS control plane has to be used
Traffic Engineering with Segment Routing

- We enhance a SDN controller with TE/SR modules
- We assume that the SDN controller is requested to allocate a set of traffic flows with a specified bit rate
  - The flow assignment algorithm is first executed in order to compute the TE paths
    - We implemented a modified version of the heuristic proposed in a previous work that tries to minimize the overall network crossing time
  - Then, for each TE path, the corresponding SR path is calculated
    - SR path is the list of segment IDs that should be added to incoming packets for instructing them through the assigned TE path
    - We propose a simple SR assignment algorithm that minimize the number of required segment IDs
Implementation and tests

- The proposed network architecture has been implemented and tested (source code is available)

- Experimental analysis with two main goals:
  - testing the SR assignment algorithm
    - 153 nodes, 354 links, 940 out of 2460 flows
  - testing the overall implementation of the solution
    - both control and data planes

![Graph showing TE paths and SR paths](image)

![Graph showing TE computation time and SR computation time](image)